Design of SAR ADC with Monotonic Capacitor Switching Scheme in 0.18µm CMOS Technology

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ABSTRACT

Analog-to-digital converter is broadly used in electronic systems. The successive-approximation-register (SAR) ADC is very popular for systems that require high speed, low energy, and more accurate analog-to-digital converters (ADCs). Due to size scaled down feature of CMOS transistors and its advantages the SAR ADCs can be designed for a range of sampling rates from MS/s to GS/s with 5 to 12 bits resolutions. Having low cost and power the SAR ADCs can have very advantages in analog processing systems specially for some low power portable devices. Many switching methods have been used in research work of ADCs. These methods have the issue of increased digital power. This paper presents SAR ADC having low power with the use of monotonic capacitor switching method in 180 nanometer CMOS technology. It is an 8-bit SAR ADC having sampling rate of 1-MS/s. The given switching method has reduced the switching energy due to small number of switches used by the architecture. Also, total capacitance is reduced by 50% due to small number of unit capacitors compared to conventional procedures. The comparator designed for this work is a high speed, low power and highly efficient. Bootstrapped switch is used as sample and hold circuit with high linearity. The ADC consumes low power of 410nW. The power consumption of comparator, DAC and SAR Logic is 19.5nW, 89.43nW and 300.6nW respectively. The ADC achieves signal-to-noise-and distortion ratio of 45.1 dB with low power consumption having ENOB of 7.2 bits. At supply voltage of 1-V and total capacitance of 2.56 pF the ADC has efficient performance having low noise.

Keywords: ADC, SAR, CMOS, S/H

1. INTRODUCTION

Different Electronic and communication systems have the requirement of low power, high bandwidth, and high-speed ADCs. Due to advancements in technologies and circuit design techniques, the successive approximation ADCs can be used for different applications including wireless sensor networks and biomedical applications [5]. For medium sampling rate and medium resolution, pipelined ADCs are mostly used, but due to the requirement of several operational amplifiers in pipelined ADCs, results in large power consumption. Also, the high-performance amplifier is a challenging task. Also, it needs large sampling capacitance for high signal-to-noise ratio because of limited signal swing. However, to have high SNR it needs sampling capacitance of small value. Due to the advantages of low power, low area requirement and low-cost, SAR ADCs are more attracting than other architectures in nanometer scaled CMOS technologies.

This paper presents design of 8-bit 1MS/s synchronous ADC. The architecture is based on monotonic capacitor switching procedure [2],[3],[4],[7],[10] that consumes low power. The proposed design has decreased the power consumption by 60-70% without the addition of any capacitor or switch. Also, it has reduced the total capacitance by 50%. This paper also gives the necessary and efficient blocks design to keep away the linearity degradation.

The remaining part is arranged as given. Section 2 gives the architecture. Section 3

gives circuit building blocks. Section 4 presents conclusions and results.

2. ARCHITECTURE

The proposed SAR ADC has used capacitor array based on binary weighted mechanism with switches, comparator, bootstrapped switch, and SAR Logic control. The capacitor array based on binary weighted has been used instead of capacitor array C-2C based to have high linearity [3]. The ADC has used a fully differential methodology to have less supply noise and a good system of common mode noise rejection. In this architecture, bootstrapped switch is used. It acts as a circuit of sample-and-hold (S/H) [6]. The ADC operates on both sides due to its differential nature. But only the operation of positive side of conventional SAR ADC is explained for concept. The bottom plates of capacitors are charged to V_{ip} during sampling phase whereas the bottom plates are readjusted to common mode voltage. Only capacitor of larger value is connected to ground. For bits decision to be one or zero, the comparator does the first comparison. If value of V_{ip} is more than V_{in}, B_1 (most significant bit) is 1. If not, B_1 is 0, and capacitor having largest value is re-switched to ground. After that C_2 is switched to $V_{ref,}$ and comparison is again performed by the comparator. The procedure is repeated till decision of LSB (least significant bit). This method is simple but not energy efficient.

Fig.1. gives architecture of given SAR ADC. Downward switching has used for fast reference settling, although it can be upward or downward. Bootstrapped switches are used to sample input signal on top plates of the capacitors. Due to this, the ADC has very high settling speed, high linearity [8] and reasonable input bandwidth. The bottom plates of the capacitors are reset to V_{ref}. Then after bootstrapped switches are switched off by ADC and first comparison is performed by the comparator without switching any capacitor. Then according to the resulted output of comparator, the capacitor C1(largest one) is shifted to ground and the other remains unchanged. The procedure is repeated until decision of the LSB. For each bit cycle only one capacitor is switched, so the power consumption is reduced.

There are several advantages of the given procedure over the conventional one. In the given architecture, the switching has no need of upward transition, so the DAC has fast settled. Also, no switching is needed for first comparison. Also, the architecture has only half number of unit capacitors as compared to conventional one.

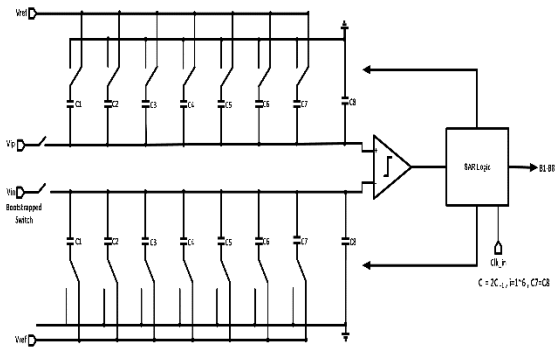

Figure 1: Proposed SAR ADC

3. CIRCUIT BUILDING BLOCKS

The key building blocks of the presented ADC includes a S/H, dynamic comparator, capacitor array, and SAR control block. Each block is given below.

A. S/H Block

In the given ADC, bootstrapped switch is used as sample and hold block [1]. To ensure linearity bootstrapping is used. Using the bootstrapped switch and keeping the voltage from gate to source of the sampling transistor at supply voltage V_{dd} results in small on resistance and high

linearity. A single-phase clock (Clks) is applied to the bootstrapped switch to on and off having a sampling capacitance of 500fF. With bootstrapping the linearity of switch has increased, results in fast settling and large input bandwidth. Also, some other switches may be combined to achieve higher precision and accuracy depending on the required performance parameters. The circuit of bootstrapped switch used is given in Fig.2.

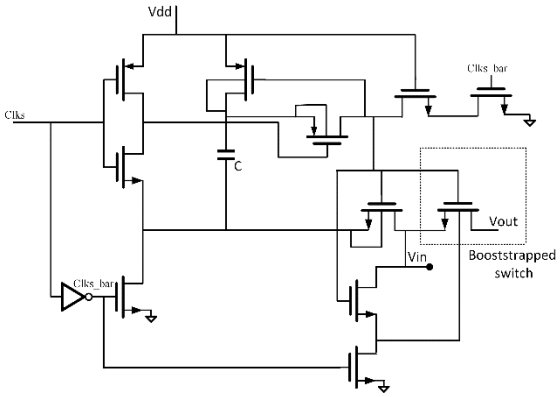

Figure 2: S/H Circuit

B. Comparator

The circuit of comparator is given in Fig.3. It has an input pair of p type transistors. The comparator operates with in input common mode voltage having ranged from V_{ref} to ground.

The comparator operates with a clock Clkc. Both outputs Out_p and Out_n are high at high Clkc. When Clkc is low, comparator compares input voltages and results one output as high with respect to the high input voltage. A biased transistor is cascaded to maintain the linearity without disturbing the power consumption or the comparison speed. The comparator has no consumption of any static current, so this comparator is good for less energy consuming architecture [9].

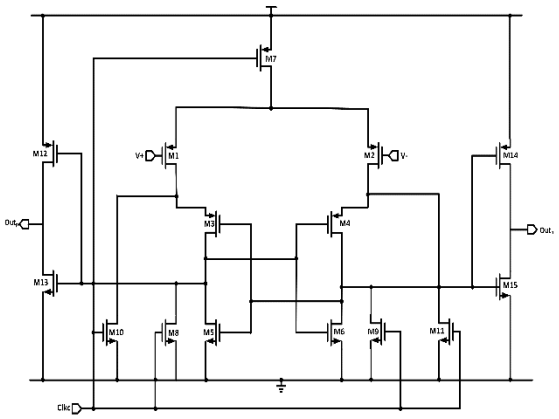

Figure 3: Comparator

C. CAPACITOR ARRAY

The given ADC has the use of binary weighted capacitor array. The unit capacitor used is 50fF. Because of small unit capacitance the ADC is very efficient. Also, the settling time is reduced. The capacitor array is shown in Fig.1.

D. SAR LOGIC

SAR logic based on synchronous logic [3] is used for given SAR ADC. This logic generates some of the necessary clocks itself internally. Clks operates the sampling switches. The sampling interval is kept as 20% of whole clock period applied. Clock Clkc is generated which is used to control the comparator. The output's Clk1 to Clk8 are used to control the capacitor array and for sampling the digital codes of the comparator. Diagram of the SAR logic is given in Fig.4.

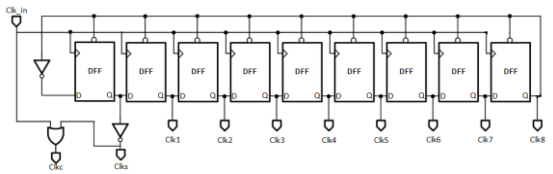

Figure 4: SAR Logic

E. DAC CONTROL SWITCH

DAC control switch consist of a static D-flipflop. Clk_i and Out_p/Out_n are applied as inputs to D-flip flop. The flip flop is proceeded by a transistor pair having

switching voltages of V_{ref} and ground. At the high output the corresponding capacitor is switched from reference voltage to ground, whereas at low output the capacitor is switched to V_{ref} [3]. Circuit of DAC switch is given in Fig.5.

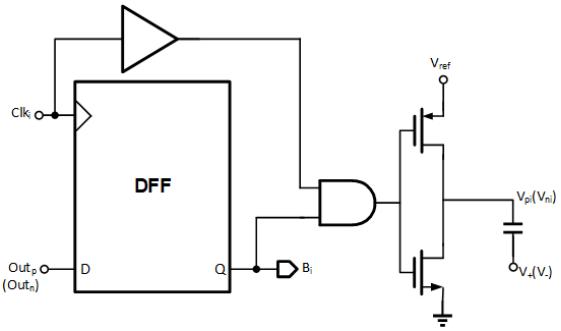

Figure 5: DAC Control Logic

4. CONCLUSION AND RESULTS

The SAR ADC is designed for applications based on low power consumption. It has used monotonic switching procedure technique for switching. Different blocks designed have been given with their simulation results. The given ADC is energy efficient, high speed and more precise as compared to conventional. The parameters of the given SAR ADC are given in table 1. The output waveforms of all blocks designed in cadence are given below.

Table 1: Parameters Table

Parameters	Value
Peak-to-Peak Voltage	1V
Sampling frequency	1MHz
Common Mode Voltage	0.5V
Sampling Capacitance	500fF
Power	410nW
SNDR	45.1 dB
ENOB	7.2 bits

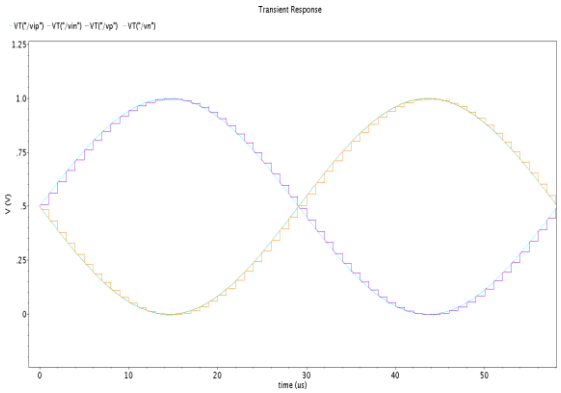

Figure 6: S/H Output

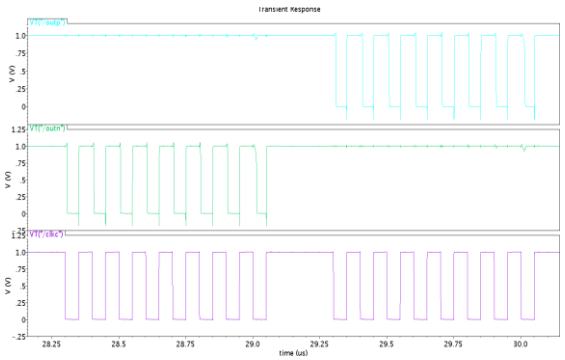

Figure 7: Comparator Output

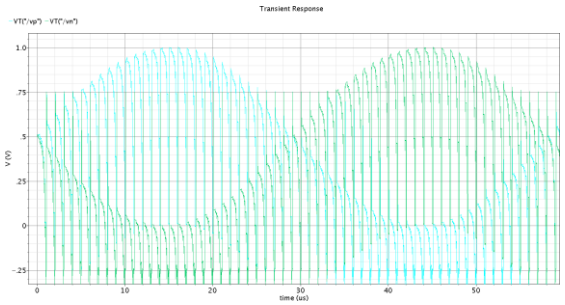

Figure 8: DAC Output

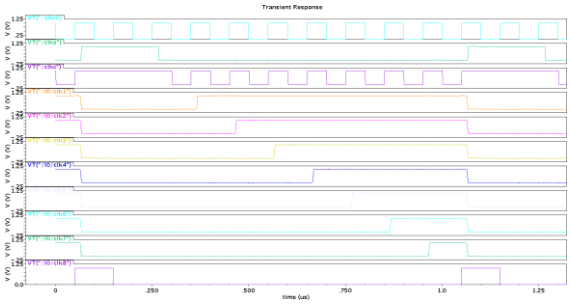

Figure 9: SAR Logic Output

5. REFERENCES

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