Inverter Based Delta-Sigma Modulator for Microphone Sensor

Saeed Ullah, Arshad Hussain
Department of Electronics, Faculty of Natural Sciences
Quaid-i-Azam University, Islamabad 45320-Pakistan
Islamian537@gmail.com, arshad@qau.edu.pk

ABSTRACT

This paper presents a single-bit second-order switched-capacitor delta-sigma modulator for microphone sensor applications of signal bandwidth of 10 kHz. The modulator structure performance optimized with the noise transfer function (NTF) and signal transfer function (STF). To reduce the power of the modulator a power-hungry operational amplifier-based integrator replaced by low power inverter-based integrator. A cascade of multiple feedforward architecture adopted to reduce the swing inside the loop filter to process only the quantization noise. The adder in front of the quantizer optimized for smaller swing so that quantizer can also be utilized as an amplifier. An inverter-based integrator designed with power consumption of 9.5 µW at supply voltage of 350mV. It implements DC gain of 18.8dB with GBW of 48 MHz. The proposed second-order single bit delta-sigma modulator evaluated for different oversampling ratio (OSR) of 64, 128, 256 and 512. The modulator with ideal integrators can achieve higher resolution for out-of-band gain (OBG) of 1.5, 2, 2.5 and 3 for signal bandwidth of 10 kHz. Also, the NTF zero optimization results in much higher performance as compared without zero optimization. Finally, the inverterbased integrator will be utilized as integrator in the loop filter of the proposed deltasigma modulator and performance will be evaluated for high resolution.

Keywords: Inverter-based amplifier, Signal Transfer Function, Analog-to-Digital Converter, Switched-Capacitor, Noise Transfer Function.

1. INTRODUCTION

Power reduction of the analog circuit quite challenging with reduced supply voltage. While due to the scaling of CMOS technology, digital circuit can take advantage due to reduced supply. The key building block of analog circuit is the operational transconductance amplifier (OTA) that is the main bottleneck for the reduction of supply voltage and power dissipation [1]-[9]. Due to the MOS threshold voltage is not scaled as much as supply voltage due to leakage current consideration that limits the application of traditional OTA to low voltage environment. And the supply voltage reduction that directly affects the amplitude of the processed signal in OTA. Therefore, the design of analog circuit in nanometer CMOS technology poses challenges. Low voltage OTA have been explored, but the supply voltages of the OTA restricted and have reached the limits of further scaling, because they are strictly limited by the input commonmode voltage [10]-[11]. Analog to digital converter (ADC) function as basic building block for analog circuits. Due to smaller supply voltage analog circuit performance degrades, finally results in lower signal-to-noise ratio. The switchedcapacitor circuits easily simulated, insensitive to clock jitter as long as full settling occurs. The pole zero locations set adjusted by capacitor ratio, which are highly accurate. Delta-sigma modulator ADC uses noise shaping and oversampling to achieve higher performance. Many circuit design techniques have been investigated to overcome the

challenge of CMOS technology scaling. Considering an OTA with body-driven OTA, a continuous-time (CT) third-order modulator presented with no internal voltage boosting. It uses active RC integrators. The ratio between the resistors set the CT modulator coefficient. The modulator implemented as fully differential structure to reduces the distortion due to asymmetries between rising and falling edges of digital to analog (DAC) signal [12]. A comparator-based switched-capacitor circuit technique presented for the scaled CMOS technologies. The implementation of comparator-based circuit with comparator and current source. It works like during charge transfer, the comparator detects the virtual ground condition in place of OTA, that normally forces the virtual ground condition. The proposed techniques implemented in 0.18um CMOS. It can achieve an effective number of bit (ENOB) of 8.6 bits for a 3.8 MHz input signal and dissipates 2.5 mW [13]. An inverter also considered to be an alternate for OTA in a low-voltage design. The input transistor of the inverter operates in a subthreshold region in steady state, so the inverter can operate at very low supply with small static current. Also, when the inverter enters in the slewing period, one of the two input transistors is turned on, while the other one is off. Therefore, a high slew-rate obtained with minimum shortcircuit current. Also, the dc gain of the traditional class-C inverters is below 60 dB, that causes leakage and nonlinearity [14] [15].

This paper proposed CIFF second-order modulator for low supply voltage, high dynamic range modulator for signal bandwidth of 10 kHz for oversampling ratio (OSR) of 128. The modulator can achieve signal-to-noise ratio of 40 dB with power dissipation of 18.8nW at supply voltage of 350 mV with common mode voltage of 100mV. After the introduction, the second section discuss the structure of the modulator design, while the third section describes the modeling and simulation of the modulator and explain the circuit nonidealities for switched-capacitor implementation. Finally, the section four concludes the paper.

A I cascade of integrator with multiple feed

Parameter	Values
a1	1.7370
a2	0.8074
b1	1
b2	0
b3	1
c1	1
c2	1
SNR	91 dB

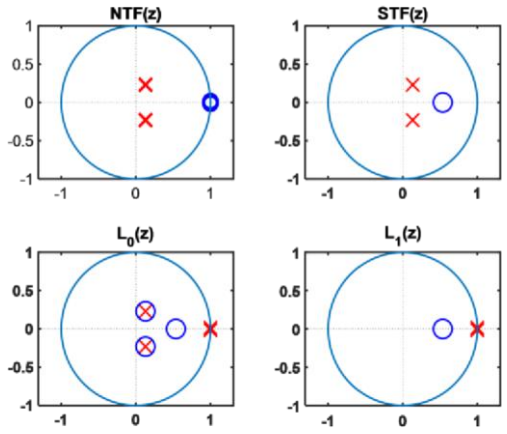

Figure 1: Poles zeros plot for STF and NTF

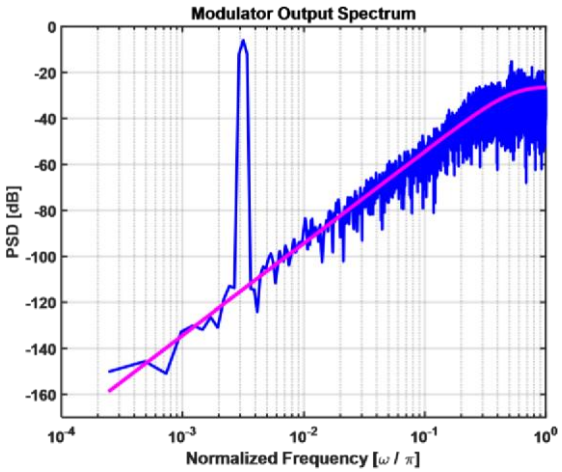

Figure 2: Output PSD plot

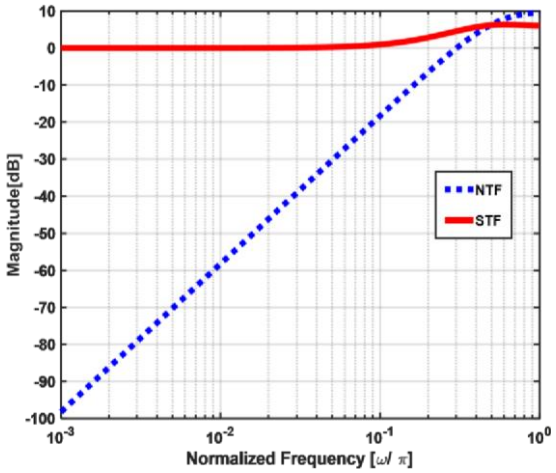

Figure 3: STF and NTF plot

forward (CIFF) second-order modulator for single bit design proposed for signal bandwidth of 10 kHz. The modulator performance optimized using tuning the modulator. The modeling of the modulator performed using DeltaSigma Toolbox [13]. The out-of-the-band gain (OBG) of the modulator raised to improves the performance of the modulator. The proposed CIFF modulator uses OBG of 1.5, 2, 2.5 and 3 for oversampling ratio of 128. The higher OBG results in more shaping of quantization noise Table I shows the performance of the second-order single bit modulator coefficient for OBG = 1.5 and ideal modeling signal to

rcle in the z-domain. The zeroes of the NTF lies on the DC while poles lie inside the unit circle for higher stability of the modulator. Due to zeros at the DC of the unit circle, the maximum quantization noise suppression is possible. Also, as the integrator poles at the unity that result in maximum quantization noise suppression. The output power spectral density (PSD) shown in Figure 2 as quantization noise shaped as high pass filter due to high pass filter feature embedded inside the modulator. Figure 3 shows the STF and NTF plot of the modulator. The dotted line shows the NTF plot as high pass function. While the constant line shows a low pass filter with peaking shows at the end. The CIFF modulator structure have STF peaking embedded inside the modulator. The CIFF architecture allow much smaller swing inside the loop filter due to signal is feedforwarded at the front of the quantizer. The signal directly forwarded to the quantizer while the noise is processed by the integrator inside the loop filter. The DC gain requirement of the operational amplifier (op-amp) is much relaxed due to smaller swing inside the loop filter. Figure 4 shows the swing at the output of both integrators.

noise ratio (SNR) of 83 dB. As the OBG further increased to 2, the SNR performance further improves to 88 dB as shown in Table II. In the Table III, the OBG is set to 3 to improves the performance to 91 dB. Due to the low pass features of the proposed modulator, the STF shows constant response at low frequencies while NTF shows high pass filter behavior by shaping more quantization noise at high frequencies. All integrator has operational amplifier (op-amp) with infinite gain and maximum quantization noise suppression.

Figure 1 shows the STF and NTF plot of the modulator as well as loop filter zeroes and poles location on the unit

2. SWITCHED-CAPACITOR CIRCUIT MODELING AND SIMULATION

To realize the switched-capacitor implementation of the second-order single bit modulator, Cadence specture used for modeling of CIFF structure of the modulator. All integrators are simulated in the Cadence using inverterbased integrator, used as three stage integrators with open loop dc gain of 18dB and GBW of 48MHz. Each integrator has power consumption of 9.4nW. Hence, the total power consumption of the complete modulator excluding switches and comparator is 18.8nW. With all switches of the implementation considered to be ideal and comparator is also ideal , the Table V shows the performance of the modulator with different OSR and SNR respectively. The output PSD plot with OSR of 128 can achieve SNR of 41 dB for signal bandwidth of 10 kHz.

3. CONCLUSION

A second-order single-bit delta-sigma modulator modeling and switchedcapacitor implementation presented for microphone sensor. The modulator can achieve 41dB SNR at the switchedcapacitor implementation. All the integrator implemented using

inverterbased amplifier. An inverter-based amplifier has dc gain of 18.8 dB with GBW of 48 MHz. The modulator system level modeling and simulation performed for inverter-based amplifier. The modulator consumes power of only 18.8nW at the supply voltage of 350 mV with common mode voltage level of 100mv.

4. ACKNOWLEDGMENT

This research work was supported by University Research Fund (URF 20182019) of Faculty of Natural Sciences, Quaid-i-Azam University, Islamabad, Pakistan.

5. REFERENCES

[1] **Y. Chae and G. Han, 2009,** Low voltage, low power, inverterd-based switched-capacitor delta-sigma modulator, IEEE Journal of Solid-State Circuits, 44(2), pp. 458-472.

[2] **S.S Rajput et al., 2002,** Low voltage analog circuit design techniques, IEEE Circuits Syst. Mag., 2(1), pp. 24-42.

[3] **S. Chatterjee, Y. Tsividis, and P. Kinget, 2005**, 0.5-V analog circuit techniques and their applications in OTA and filter design, IEEE Journal of Solid-State Circuits, 40(12), pp. 2373-2387.

[4] **F. Michel and M. S.J. Steyaert, 2012,** A 250 mV 7.5uW 61 dB SNDR SC ΔΣ modulator using nearthreshold-voltage-biased inverter amplifiers in 130nm CMOS, IEEE Journal of Solid-State Circuits, 47(3), pp. 709-721.

[5] **H. Roh et al., 2009,** A 0.6-V delta-sigma modulator with subthresh-oldd-leakage suppression switches, IEEE Trans. Circuits Syst. II, Exp Briefs, 56(11).

[6] **M. G. Kim et al., 2008**, A 0.9 V 92 dB double -sampled switchedRC delta-sigma audio ADC, IEEE Journal of Solid-State Circuits, 43(5), pp. 1195-1206.

[7] **N. Maghari et al., 2006,** DSturdy MASH delta-sigma modulator, Electron. Lett., 42(22), pp. 12691270.

[8] **K. Cornelissens and M. Steyaert, 2008**,Design Consideration for Cascade ADC's , IEEE Trans. Circuits Syst II, Exp. Brifes, 55(5), pp. 389-393.

[9] **Hao Luo, Yan Han, Ray C.C. Cheung, Xiaopeng Liu and Tianlin Cao, 2013**, A 0.8-V 230uW 98-dB DR Inverter-Based Modulator for Audio Applications, IEEE Journal of Solid-State Circuits, 48(10), pp. 2430-2441.

[10] **L. Yao, M.S.J. Steyaert, and W. Sansen, 2004,** A 1-V 140 μW 88dB audio sigma-delta modulator in 90nm CMOS, IEEE Journal of Solid-State Circuits, 39(11), pp. 18091818.

[11] **J. Goes, B. Vaz, Monteiro, and N. Paulino, 2006,** A 0.9 V modulator with 80 dB SNDR and 83 dB DR using a single-phase technique, IEEE International Solid-State Circuit Conf. Dig. Tech.pp.74-75.

[12] **K.-P Pun, S. Chatterjee, and P. Kinget, 2006**, A 0.5-V 74-dB SNDR 25 kHz CT ΔΣ Modulator with return-to-open DAC, IEEE International Solid-State Conf. Dig. Tech, pp. 72-73.

[13] **S. Norsworthy, Richard Schreier, G.C.Temes, 1997**. Delta-Sigma Data Converters Theory, Design, and Simulation, Johan Wiley & Sons, Inc., Hoboken, New Jersey. 0.5-V Bulk-driven OTA and its applications, International journal of circuit theory and applications, 43, pp. 187-204.

[14] **R. Scherier** Delta-Sigma Toolbox ((http://www.mathworks.com/matlancentral/fileexchange/19delta-sigma-toolbox).

[15] **S. Brigati** SDToolbox (http://www.mathworks.com/ma tlabcentral/fileexchange/2460-sdtoolbox).