Four-Stage Switched-Capacitor Boost Converter for MFC Cell

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ABSTRACT

This paper presents a four-stage switched capacitor based voltage doubler designed in 28nm CMOS Technology. The output voltage of the MFC is 100 mV, the proposed Switched-Capacitor converter can boost the 100mv to 1.47 V. The converter uses non-overlapping clock with frequency 50 MHz. The first stage sampling capacitor is 20 pF while the output stage capacitor is 1 pF with large resistor of 10 MHz. The proposed design utilizes four blocks of the similar types. The switched-capacitor implementation with ideal switches and ideal capacitor shows performance enhancement. The input voltage to the boost converter is 100 mV while the first stage output shows 196 mV. Which is almost double to the 100 mV. While second stage voltage doubler output is 375 mV, that is almost double to the 196 mV. The third stage output is 737mV, which is almost double to the 375 mV. The final boosted voltage at the output of the last stage is 1.47 V. The performance of the boost voltage can be improved by sizing of the capacitor size. The switches can be replaced by the NMOS and PMOS transistor and their resistance can be adjusted accordingly to meet the requirements. The circuit simulation in Cadence shows that the proposed switched-capacitor dc-dc converter can achieve 1.47 V at the output

Keywords: Switched-Capacitor, Voltage Double, MFC, Circuit, Transistor

1. INTRODUCTION

A four-stage voltage doubler utilized to implement a boost converter for MFC application. The boost converter implements four different stages to enhance the voltage coming from MFC Cell. The complete boost converter can achieve 1.47 V at the output. Design method of CMOS Voltage doubler is presented in a paper. To check performance of this design we used test bench circuits. Many equations are presented which area related to design parameters of performance. Steady state and transient behavior consider in this set. During transistor sizing many energy losses which are known such as conduction and switching losses are considered. Through electrical simulations characteristics of pump capacitors are analyzed. AMS design at 0.35 µm based examples is proposed [1]. To get DC output voltage more from the input voltage a cascade voltage doubler circuits are considered till more than 8 decades. Different voltage doubler cascade topologies are examined in presented paper. For voltage doubler cascade technology, we presented a new circuit configuration. For same no. of stages, circuit produce a good output quality and higher DC voltages as compared to conventional cascade voltage doubler [2]. To get maximization in power density and efficiency of fully differential SC based DC-DC converters is presented in presented paper. Circuit design methods are presented to permit simplified gate drivers while supporting multiple topologies. All this is designed in 0.374mm^2 SOI process. Through proof of converter prototype this method is verified. From 2-volt input supply support output voltages of 0.5 to 1.2 volt. This

attains efficiency of 79.76% at power density of 0.86 W/mm^2[3]. This paper presented regulated charge pump circuit. The power supply is 3.3 volt and design in 130nm technology. Through decoupling start up time and output ripple, this charge pump provides an automatic pump control mechanism which gives fast start up and small ripple output voltage. This is based on two different mechanism one is automatic pumping current control and other is frequency control. To Minimize ripple voltage according to output voltage current control method adjust size of this pumping driver automatically. Frequency control changes pumping period by controlling a voltage controlled oscillator. As we control input bias voltage of Voltage control oscillator the frequency of VCO at output changes from 400KHz to 600KHz. Power supply voltage is applied to this circuit is 3.3 volt while value of flying capacitor is 330nF. This will give output of 4.5 volt while gives 30mA of load current. The value of measured output ripple voltage is smaller than 33.8mV while the load capacitor is of capacitance 2F. This will cover the area of 0.25mm^2. At 1 to 30 mA range of load current, power efficiency greater than the 70%. An analytical model is presented demonstrating reasonable agreement with SPICE simulation results for recovery time and ripple voltage [4]. In another paper proposed SC voltage double using Pseudo continuous control. To regulate continuously output of doubler, this PCC don't require extra power. So, area of chip is also saved. This allows to work at low frequency without any loss of transient response. Reducing switching power loss efficiency of regulated doubler can be increased. To implement controller 3 stage op amp including time multiplexed increase active feedback compensation is designed. The design technique increased speed of loop response thus make better changes in load transient response of regulated doubler. This is fabricated in 06 micrometer CMOS technology. This will attain power efficiency more than 87% while load current is just 5mA. This doubler will operate at switching frequency of 200KHz and value of capacitor at output is 2.2 micro-Farad. This will get output ripple of 20 millivolt while load current is from 50 to 150 mA. Output transient recovery time of regulated doubler is ~25us while load current step changes of 100 mA/1us [5]. A SC based DC DC voltage converter design in 45nm. SOI CMOS hold on chip trench capacitors to attain 90% efficiency. The conversion frequency is 100MHz and get output of 2.3A/mm^2 while applied input is from 2 to 0.95 volt. Operation are explained of step up as well as step down modes. Self regulation capability allows more efficiency improvement after combining with stacked voltage domains. [6]. In this paper we proposed a SC DC DC converter which is completely integrated on chip. The input voltage is 5 volts while power supply voltage is 2.2 and 3.2 volt. This gives maximum of load current of 8mA at outputs. Two to one converter blocks are used in whole converter system. From Two to one Up converter, we attain upper output voltage and from two to one-dw converter we generate lower output voltage. As 2 to 1_up converter is not more sensitive to bottom plate parasitic capacitance loss, they are designed with MOS capacitors, which gives higher capacitance density than MIM capacitors while they have bigger bottom plate parasitic capacitance ratio. The presented design saves area and quiescent currents for control blocks while each block share needs digital and analog control blocks. The presented converter is fabricated using high voltage. This is designed in 0.35µm BCDMOS process. By using Digital control oscillator and 18 bit

shift register output voltages are regulated by means of pulse frequency modulation. This converter attain efficiency of 70% while peak efficiency is 71.4%. The output power range is from 5.4 mW to 43.2 mW. Ten phase interleaving methods enables output voltage ripples of both these outputs <1% [7].

This paper proposed a four-stage switched-capacitor based voltage doubler designed in 28nm CMOS Technology. The output voltage of the MFC is 100 mV, the proposed Switched-Capacitor converter can boost the 100mv to 1.47 V. The converter uses non-overlapping clock with frequency 50 MHz. The first stage sampling capacitor is 20 pF while the output stage capacitor is 1 pF with large resistor of 10 MHz. The proposed design utilizes four blocks of the similar types. The switched-capacitor implementation with ideal switches and ideal capacitor shows performance enhancement. The input voltage to the boost converter is 100 mV while the first stage output shows 196 mV. Which is almost double to the 100 mV. While second stage voltage doubler output is 375 mV, that is almost double to the 196 mV. The third stage output is 737mV, which is almost double to the 375 mV. The final boosted voltage at the output of the last stage is 1.47 V. The performance of the boost voltage can be improved by sizing of the capacitor size.

After the introduction, the second section discuss the design of the switched-capacitor design using cadence virtuoso, while the third section describes the modeling and simulation results and explain the circuit for the voltage doubler implementation. Finally, the section four concludes the paper.

2. Circuit Design

A switched capacitor with four switches and two capacitors designed using cadence virtuoso [3]. The switches are implemented using NMOS transistor for smaller swing while for higher swing these switches are implemented using transmission gate. The Figure 1 shows the very simple voltage doubler circuit. The switch S1 and S2 are using the same phase while the switch S3 and S4 also using same clock phase. The nonoverlapping clock are the base for the voltage doubler circuit. The nonoverlapping clock can be designed using transistor level implementation considering the clock of the system.

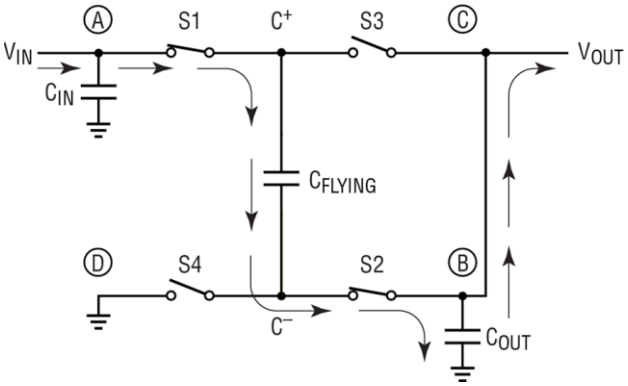

Figure 1: voltage double

3. RESULTS & DICUSSION

A switched-capacitor boost converter design for MFC application. The converter implements four stage doubler mechanism with switches and capacitor to boost the voltage and reached the output voltage more than 1 V. The switched-capacitor implementation with ideal switches and ideal capacitor shows performance enhancement. The input voltage to the boost converter is 100 mV while the first stage output shows 196 mV. Which is almost double to the 100 mV. While second stage voltage doubler output is 375 mV, that is almost double to the 196 mV. The third stage output is 737mV, which is almost double to the 375 mV. The final

boosted voltage at the output of the last stage is 1.47 V. The performance of the boost voltage can be improved by sizing of the capacitor size. The switches can be replaced by the NMOS and PMOS transistor and their resistance can be adjusted accordingly to meet the requirements.

4. CONCLUSION

A four-stage switched-capacitor boost converter designed using voltage doubler. The circuit simulation shows the proposed design can achieve output voltage of 1.47 at the last stage output. The proposed design utilizes four blocks of the similar types. The switched-capacitor implementation with ideal switches and ideal capacitor shows performance enhancement. The input voltage to the boost converter is 100 mV while the first stage output shows 196 mV. Which is almost double to the 100 mV. While second stage voltage doubler output is 375 mV, that is almost double to the 196 mV. The third stage output is 737mV, which is almost double to the 375 mV. The final boosted voltage at the output of the last stage is 1.47 V. The performance of the boost voltage can be improved by sizing of the capacitor size. The switches can be replaced by the NMOS and PMOS transistor and their resistance can be adjusted accordingly to meet the requirements. The circuit simulation in Cadence shows that the proposed switched-capacitor dc-dc converter can achieve 1.47 V at the output

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6. REFERENCES

[1] **L. Rodriguez, et al, 2016**, Design of CMOS cross-coupled voltage doubler, IEEE ANDESCON, Arequipa, Peru.

[2] **A. Toudeshki, et al, 2013,** Development of a New Cascade Voltage-Doubler for Voltage Multiplication, Chinese Journal of Engineering, Hinawi.

[3] **H. Le, et al, 2011,** Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters, IEEE Journal of Solid-State Circuits, 46(9), pp. 2120-2131.

[4] **J. Lee, et al, 2006,** A regulated charge pump with small ripple voltage and fast start-up, IEEE Journal of Solid-State Circuis, 41(2), pp. 425-432.

[5] **H. Lee, et al, 2007,** An SC Voltage Doubler with Pseudo-Continuous Output Regulation Using a Three - Stage Switchable Opamp, IEEE Journal of Solid-State Circuit, 42(6), pp. 1216-1229.

[6] **L. Chang, et al, 2010,** A fully integrated switched-capacitor 2:1 voltage converter with regulation capabiity and 90% efficient at 2.3A/mm2, Symposium on VLSI Circuit, USA.

[7] **H. Jeon, et al, 2012,** A fully integrated switched-capacitor DC-DC converter with dual output for low-power applications, IEEE Tran on Circuit & Syst-II, 67(9), pp. 1649-1653.