CMOS Operational Amplifier with Gain Booster

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ABSTRACT

This paper presents a two-stage operational amplifier with folded Casecode as single stage and common source amplifier as second stage at supply of 1.2-V in 0.18 µm technology. The amplifier uses gain booster to improve the gain of the first stage amplifier. The folded cascade allows much higher swing at the output. The proposed design allows to optimize with maximum gain. The implemented design has NMOS differential pair as an input differential gain stage. The first stage tail current is 59 µA. While the second stage each branch current 4.5 uA. The gain booster 6.23 nA on each side. The overall power consumption is 82 µW at supply voltage. There is a trade-off speed, power, supply voltages. High DC gain is important factor of the op-amp to achieve the high gain second stage is implemented which achieved 44 dB gain and power consumption of the second stage is 82 µW. The operational amplifier first stage has DC gain of 26 dB, while second stage have DC gain of 44 dB. The proposed design can be used pipeline ADC due to high precision applications requirement. The overall DC gain of the multi-stage amplifier with gain booster have open loop DC gain of 72 dB and phase margin of 67 degree with power consumption 82 µW.

Keywords: op-amp, multi-stage op-amp, DC gain, GBW, output swing

1. INTRODUCTION

Recent trends to package analog and digital building block of CMOS technologies allow for integration on an integrated chip increased. Due to the large demands on portable electronics devices with higher battery life. These portable devices require large number of analog circuits with low power consumption [1]. An operational amplifier is main part of the analog circuit. There are many topologies to design op amp [2]. To achieves the high gain with minimum power consumption. The implemented design presents a fully differential two-stage operational amplifier with folded cascade as first stage and common source amplifier as second stage at supply of 1.2-Volt at 5MHZ input frequency in 0.18 µm CMOS technology. In this paper first design the single stage op-amp by using CMOS technology to achieve higher gain in this paper use the gain booster topology and implement 2nd stage of the o-amp and the design is fully differential to provide the large output swing. The paper consists of three sections after discussion on introduction. in section (ii) Discuss the design and implementation of folded of folded cascade op amp with gain booster topology and in section (iii) provide the simulation-based results. finally, section (iv)concludes the paper.

2. DESIGN OF TWO STAGE OPERATIONAL AMPLIFIER

The implemented design of the folded cascade [3] op-amp are shown in the

figure 1. The implemented designed of the op amp consists of three subparts, namely single stage op-amp, gain booster topology and second stage of the op-amp. The main objective of this topology to achieve high gain at low voltage the circuit level design and implementation are explained in below section

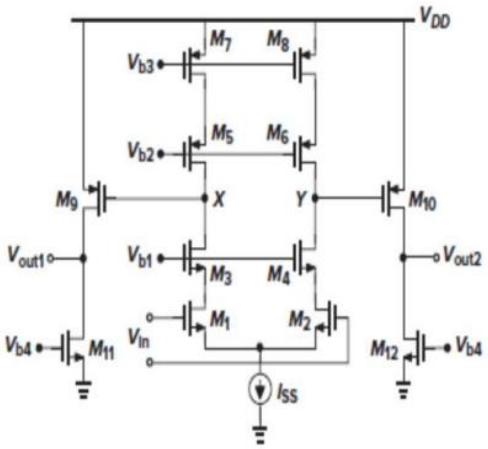
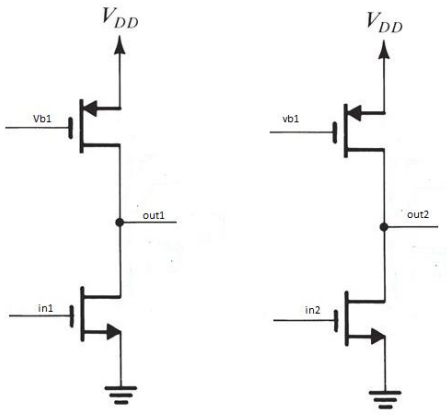


Figure 1: Two Stage Amplifier

A Design of Gain booster circuit

To improve the gain of the use Gain booster topology, improve the accuracy of the operational amplifier circuit without any loss of speed. Gain booster circuit of the op are show in figure 2



B. implementation of Single Stage op-amp

The implemented design of the single stage of the op-amp consists of PMOS and NMOS transistor. Two NMOS transistor M1, M2 are the basic differential input of the op amp. The gate of M1, M2 transistor are the positive and negative inputs with respect to transistors. At the input transistor M1, M2 differential input voltages are applied which are amplified the gain of the op amp. in this circuit use M3 and M4 transistor as active load mirror because the use of the active load provides the large output resistance the current mirror converts the dual input signal into signal input [4]. To improve the gain of the gain booster circuit were also implanted at first stage of the op amp. this stage technique reduces the feedback from the output to the drain of the input transistor thus the impedance at the output of the circuit is increased by the gain of the gain booster circuit [5]

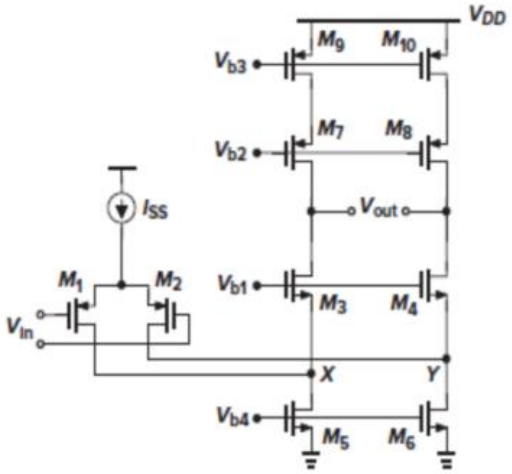


Figure 3: Single Stage Folded Cascade Amplifier

To improve the gain of the implemented the gain booster circuit of which are shown in figure 4

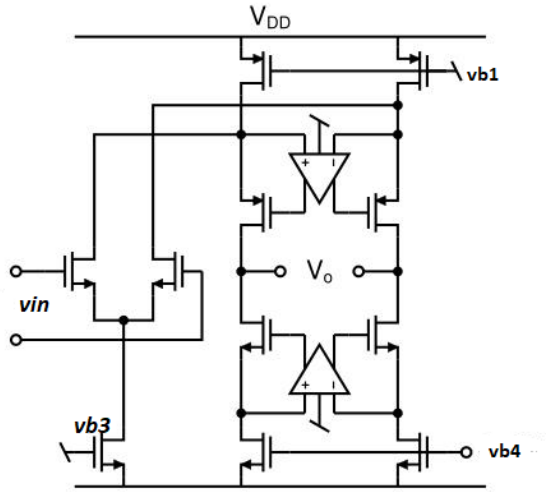


Figure4 Single stage of the op amp with gain booster circuit

C Design of second Stage of op amp

The second stage of the op amp consists on two PMOS and two NMOS transistor they provide the additional gain to the op-amp [6]. the output of single stage is connected through the transistor the configuration of the second stage of the op amp were also called the common source configuration. To maintain the stability of the needs to draw more current at second stage and use the RC circuit for stability of the op amp. Implemented design of the are shown in Figure 5

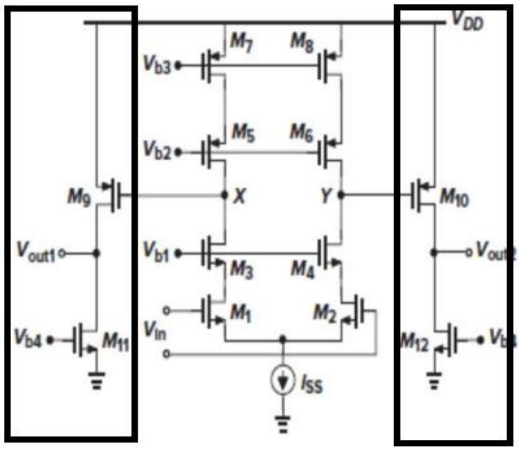


Figure 5: Second Stage of OP AMP

3. SIMULATION AND RESULTS

The design of the folded cascade op-amp was implanted at 1.2-V power supply and 5MHZ input frequency in CMOS technology. To check performance of the folded cascade perform the different analyses and then measure the performance results. As an initial stage design the single stage of the folded cascade so first simulate AC analyses and measure DC gain and phase of the margin of the single stage op amp with gain booster circuit.

4. AC ANALYSES OF THE SINGLE STAGE OP AMP WITH GAIN BOOSTER

Sinusoidal wave of 5MHZ with 1.2-volt ac supply is given at the input of the op amp then simulate the AC analyses of the op amp, Simulation result show that the implemented design of the single stage op amp achieves 55 dB DC and the phase margin of 65-degree simulation results are shown in figure 4

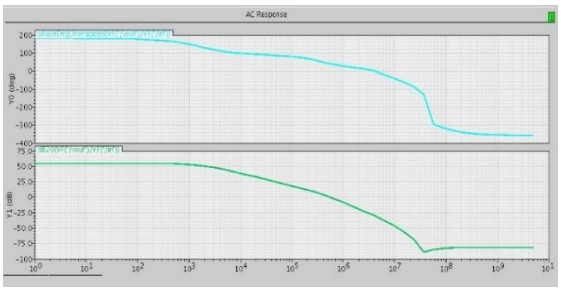


FIGURE 6: DC GAIN AND PHASE MARGIN

5. AC ANALYSES OF THE TWO STAGE OP AMP WITH GAIN BOOSTER

To improve the DC gain of the op-amp, add second stage of the op amp and then preform the AC analyses to check the performance of the op amp Simulation result show that the implemented design of the op amp achieves 72 dB DC gain and

the phase margin of 67-degree simulation results are shown in figure 7

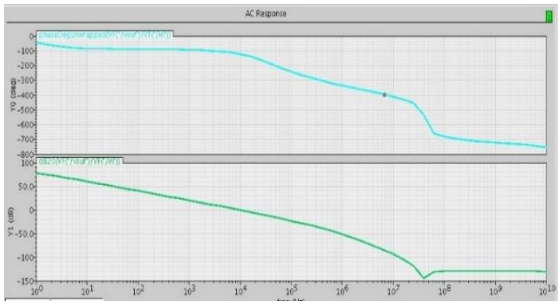


FIGURE 7: DC GAIN AND PHASE MARGIN

6. CONCLUSION

The implemented design presents the implementation of the CMOS two stage Folded Cascade op amp. the simulation results show the implemented design of the Folded cascade operational amplifier achieve required DC gain and phase margin. The implemented design operates in saturation region and regulate its bias current bias current. The implemented design of the operational amplifier with gain booster circuit achieve achieves the high gain of the 72 dB, phase margin of 67 degree and consume very low power of 82 µw.

REFERENCES

[1] **Behzad Razavi, 2017**, Design of Analog CMOS Integrated Circuits, Second EditionMcGraw Hill.

[2] **Huijsing, Johan, 2011**, Operational Amplifier: Theory and Design, Springer, 2nd Edition, ISBN 9400705956.

[3] **R. Klinke, B. J. Hosticka, and H. Pfleiderer, 1989,** A Very High Slew-Rate CMOS Operational Amplifier, IEEE Journal of Solid- State Circuits, 24, pp. 744-746.

[4] **H. Lee and P.K.T. Mok, 2001**, A CMOS Current-Mirror Amplifier with Compact Slew Rate Enhancement Circuit for Large Capacitive Load, Proc of IEEE International Symposium on Circuit and Systems (ISCAS), pp. 220-223.

[5] **R. Santos-Tavares, J. Goes, 2013**, Single-Stage Amplifiers with Gain Enhancement and Improved Energy-Efficient employing Voltage-Combiners, Proe of IFIP/ IEEE 21st International Conference

[6] **Rida S. Assaad amd Jose Sliva-Martinez, 2009**, The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier, IEEE Journal of Solid-State Circuit, 44(9), pp. 2535-2542.