A 50 dB Gain 0.5 V Bulk-Driven Amplifier

Muhammad Ahmad, Arshad Hussain, Zeeshan Akbar
Department of Electronics, Faculty of Natural Sciences
Quaid-i-Azam University, Islamabad 45320-Pakistan
m.ahmad.qau@gmail.com, arshad@qau.edu.pk

ABSTRACT

This paper presents a low power design of a bulk-driven operational amplifier in 28 nm CMOS Technology. The power efficient circuit blocks are challenging to design in nanometer CMOS Technology. The bulk driven MOS transistor have a direct relationship on the operation of differential pair. The key limitations of bulk-driven amplifier are input transconductance, which is typically three to five time smaller than the gate transconductance. It results in smaller voltage gain and results in large input referred noise, which is known to be disadvantage. To cater the possible disadvantages partial positive feedback utilized. The proposed design of bulk-driven amplifier designed without partial positive feedback for larger output swing and larger DC gain with much smaller supply voltage. It increases an overall voltage gain of the amplifier, that results in high precision. Also, common mode level at the input as well as at the output are equal. It is a two-stage circuit design with very small g_{mb}. It presents the design and analysis of a low-power, high-gain bulk-driven CMOS based operational amplifier in 28 nm technology having supply voltage of 0.5-V. The bulk-driven amplifier is designed for delta-sigma modulator to attain 10-bit resolution for the power consumption of 4 µW with DC gain of 50 dB and phase margin of 65 degree.

Keywords: Bulk-Driven Amplifier, DC gain, Phase margin, positive feedback.

1. INTRODUCTION

This paper presents a low power design of a bulk-driven operational amplifier in 28 nm CMOS Technology. The bulk driven MOS transistor have a direct relationship on the operation of differential pair. The key limitations of bulk-driven amplifier are input transconductance, which is typically three to five time smaller than the gate transconductance. Due to increasing demand of ultra-low portable systems that results in increasing interest in analog design and mixed-signal circuits, powered with much low supply voltage, even smaller than 0.5-V. These are low-voltage amplifier, linear transconductors, differential difference amplifier and many other building blocks. There are always needs to ensure sufficient voltage swing at such extreme conditions [1]. One of the very important technique is bulk-driven techniques, often considered. The bulk-driven amplifier suffers from reduced transconductance, that results in large input noise and offset. One of the most important analog building blocks in analog circuit is the operational transconductance amplifier (OTA). An ultra-low voltage operational transconductance amplifier is designed to achieve DC gain of 98 dB at supply voltage of 0.3-V in 0.18 µm CMOS Technology. The amplifier has gain bandwidth product of 3.1 kHz [1]. A more compact class AB bulk-driven amplifier is designed for supply voltage of 0.3-V in 180 nm CMOS Technology. The proposed ultra-low voltage amplifier consumes only 12.6 nW power and can achieve DC gain of 64 dB and phase margin of 52 degree with gain bandwidth product of 2.96 kHz. It can drive the capacitive load of 30 pF and common mode rejection ratio (CMRR) of

110dB [2]. An ultra-low supply voltage of 0.4V OTA design is proposed. The input stage of the proposed OTA is new stage exploiting the concept of partial positive feedback. The proposed input stage offers improvement of all basic performance metrics, including input-referred noise and offset voltage. The proposed OTA simulated in 50 nm CMOS process with power dissipation of 24 µW with open loop DC gain of 60 dB and gain bandwidth product of 2.18 MHz for 20pF load capacitance [3]. An enhanced input differential pair for low-voltage bulk-driven OTA is designed. It employs two bulk-driven flipped voltage follower cells as nonlinear tail current sources to enhance the slewing behavior. It increases the transconductace of the proposed design two time against the conventional bulk-driven input differential pair. These circuitry ideas lead to an improvement in the amplifier specification such as DC gain, slew-rate, and input noise without any degeneration in other parameters. The proposed amplifier at supply voltage 0.5V achieves dc gain 78-dB, gain bandwidth of 7.5 kHz and slew-rate of 8.6 V/ms with power consumption 46 nW [4]. A low voltage input stage constructed from bulk-driven PMOS transistor. It is based on partial positive feedback and offers significant improvement of both input transconductance and noise performance compared with those achieved by the corresponding already published bulk-driven structures. The proposed input stage offers also extended input common-mode range under low supply voltage in relevant to a gate-driven differential pair. A differential amplifier based on the proposed input stage is also designed, which includes an auxiliary amplifier for the output common-mode voltage stabilization and a latch-up protection circuitry. Both input stage and amplifier circuits were implemented with 1 V supply voltage using standard 0.35µm CMOS process, and their performance evaluation gave very promising results [5]. A bulk-driven amplifier at supply voltage of 0.5-V designed in 50nm CMOS Technology. The proposed circuit of OTA characterized for improved linearity and dynamic range obtained for transistor operating in moderate inversion region and also OTA application like voltage integrator and second-order low pass filter described. The performance parameter for the case of voltage integrator is follow, as unity gain frequency of 57-kHz to 153-kHz. The open loop DC voltage gain is 67 dB with phase margin of phase error of -0.54 degree. The total input referred noise, integrated between 1 kHz to 100 kHz is equal to 119.8 μV_{rms} [6]. A PVT insensitive bulk-driven OTA with enhanced DC gain proposed in the 65 nm CMOS Technology. A cross-coupled active load is employed at the bulk-driven input stage to enhance the gain of the OTA. A cross-forward gain stage was place between the input and output stages of the OTA to enhance the output stage transconductance. The cross-forward stage improves the phase margin of OTA and keep the amplifier stable even for large capacitive loads and also improves overall DC gain. The simulation using UMC 65-nm operates at a supply voltage of 0.5-V results in DC gain of 72 dB at very low frequency and has phase margin of 74 degree with unity gain frequency of 680 kHz. The same OTA is also simulated with supply voltage of 0.35-V and load capacitance of 20 pF, the OTA provide DC gain of 55 dB and phase margin of 68 degree at a unity gain frequency of 617 kHz. The power dissipation for both the design was 3.03 uW and 1.56 uW for supply voltages of 0.5 and 0.35-V respectively.

This paper proposed low power design of a bulk-driven operational amplifier in 28 nm CMOS Technology. The power efficient circuit blocks are challenging to design in nanometer CMOS Technology. The bulk driven MOS transistor have a direct relationship on the operation of differential pair. The key limitations of bulk-driven amplifier are input transconductance, which is typically three to five time smaller than the gate transconductance. It results in smaller voltage gain and results in large input referred noise, which is known to be disadvantage. To cater the possible disadvantages partial positive feedback utilized. The proposed design of bulk-driven amplifier designed without partial positive feedback for larger output swing and larger DC gain with much smaller supply voltage. It increases an overall voltage gain of the amplifier, that results in high precision. Also, common mode level at the input as well as at the output are equal. It is a two-stage circuit design with very small g_{mb}. It presents the design and analysis of a low-power, high-gain bulk-driven CMOS based operational amplifier in 28 nm technology having supply voltage of 0.5-V. The bulk-driven amplifier is designed for delta-sigma modulator to attain 10-bit resolution for the power consumption of 4 µW with DC gain of 50 dB and phase margin of 65 degree.

After the introduction, the second section discuss the design of the modulator design with CIFB and CIFF structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the fifth-order 4-bit quantizer for CT design implementation. Finally, the section four concludes the paper.

2. OTA DESIGN

A pseudo-differential amplifier also known as common-mode feedforward configuration. As the amplifier is supplied with non-symertical voltage source, then the input voltages are balanced around mid-supply voltage. The input voltage is applied between the bulk terminals of the diode-connected p-channel transistor thus modulating their threshold voltages. The drain voltage of these transistors are fed to the gates of the corresponding transistors in such a way controlling their drain currents. The OTA can be easily used for voltage integrator by realizing the OTA by loading the output of the

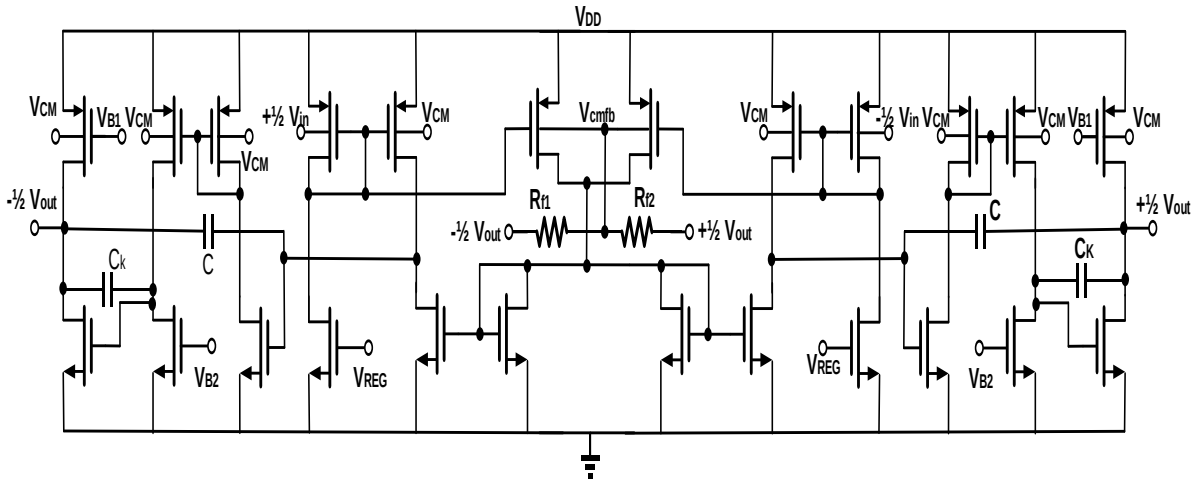

Figure 1: Bulk-Driven Amplifier

transconductance stage with linear capacitance. However, to satisfy certain frequency characteristics of the OTA-C integrator for low frequencies, the amplifier should possess sufficiently large open-loop DC voltage gain. Typically, the voltage gains larger than 60 dB is required in most of the applications. Due to low intrinsic voltage gain of MOS devices in deep submicron technologies, it is not easy to fulfill the target requirement. The proposed Bulk-Driven OTA can achieve 50 dB DC gain and phase margin of 65 degree for typical process corner (TT). While the OTA can achieve DC gain of 55 dB for FF process corner. The OTA can achieve DC gain of 52 dB for FS process corner. The OTA can achieve DC gain of 48 dB for SF process corner, While for SS process corner, the OTA can achieve DC gain of 44 dB.

3. CONCLUSION

It presents the design and analysis of a low-power, high-gain bulk-driven CMOS based operational amplifier. To cater the possible disadvantages partial positive feedback utilized. The proposed design of bulk-driven amplifier designed without partial positive feedback for larger output swing and larger DC gain with much smaller supply voltage. The bulk driven MOS transistor have a direct relationship on the operation of differential pair. The key limitations of bulk-driven amplifier are input transconductance, which is typically three to five time smaller than the gate transconductance. It increases an overall voltage gain of the amplifier, that results in high precision. Also, common mode level at the input as well as at the output are equal. It is a two-stage circuit design with very small gmb. It presents the design and analysis of a low-power, high-gain bulk-driven CMOS based operational amplifier in 28 nm technology having supply voltage of 0.5-V. The bulk-driven amplifier is designed for delta-sigma modulator to attain 10-bit resolution for the power consumption of 4 µW with DC gain of 50 dB and phase margin of 65 degree

4. ACKNOWLEDGMENT

This research work was supported by System-on-Chip Design Laboratory (SoC), Department of Electronics, Faculty of Natural Sciences, Quaid-i-Azam University, Islamabad, Pakistan.

5. REFERENCES

[1] **T. Kulej, et al, 2020,** A 0.3-V 98-dB Rail-to-Rail OTA in 0.18um CMOS, IEEE Journal of Access, 8, pp.27459-27467.

[2] **T. Kulej, et al, 2020,** A Compact 0.3-V Class AB Bulk-Driven OTA, IEEE Trans Very Large Scale Integration, 28(1), pp. 224-232.

[3] **T. Kulej ,2014,** A0.4-V Bulk-Driven Operational Amplifier with Improved Input Stage, Circuits Syst Signal Process 34, pp. 1167-1185.

[4] **Meysam Akbari, et al, 2021,** An Enhanced Input Differential Pair for Low-voltage Bulk-driven Amplifiers, IEEE Trans Very Large Integration (VLSI) systems, 29(9), pp. 1601-1611.

[5] **George Raikos, et al, 2011,** Low-voltage bulk-driven input stage with improved transconductance, International Journal of Circuit Theory and Applications, pp. 327-339.

[6] **T. Kulej et al, 2013,** A 0.5-V bulk-driven OTA and its applications, International Journal of Circuit Theory and Applications, 43, pp. 187-204.

[7] **S. Norsworthy, Richard Schreier, G.C. Temes**,1997, Delta-Sigma

Data Converter Theory, Design, and Simulation, John Wiley & Sons, Inc., Hoboken, New Jersey.